

ABSTRACT OF THE DISCLOSURE

A test pattern which is delivered from an LSI tester simulator and a corresponding test cycle number are stored in a first memory 26 while device output data which is formed by CAD data and a corresponding test time are stored in a second memory 27. The test pattern in the first memory and the device output data in the corresponding second memory are extracted by a comparing and synchronizing unit 28 and are then input to the LSI tester simulator 10. In the LSI tester simulator, the device output data is compared against expected values. If the entire device output data are in coincidence with the expected values, this test pattern is determined to be acceptable. In addition, a verification is made to see whether or not a strobe pulse which defines the determination timing for the comparison between the device output data and the expected values has occurred for all the states in the device output data.

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